TRANSISTOR WITH BOTTOMWALL/SIDEWALL JUNCTION CAPACITANCE REDUCTION REGION AND METHOD

ABSTRACT OF THE DISCLOSURE

A method of fabricating a transistor comprises forming a gate structure outwardly of a semiconductor substrate, wherein the gate structure comprises a gate, a gate insulator and sidewalls and forming source region and a drain region in the substrate using the gate structure as a mask, wherein a channel is defined in the substrate between the source region and the drain region. A bottomwall/sidewall junction capacitance reduction region extending within and between the source region and the drain region is formed, wherein the bottomwall/sidewall junction capacitance reduction region extends at least partially through the bottomwall junction or the sidewall junction.